Notice of Allowability	Application No.	Applicant(s)	
	09/871,978	HATAKENAKA ET AL.	
	Examiner	Art Unit	
	David Ton	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Amendment filed 06/14/2004 and Supplemental Declaration filed 08/23/2005*.

2. ☒ The allowed claim(s) is/are *1-7 and 10-16*.

3. ☐ The drawings filed on _____ are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☒ Certified copies of the priority documents have been received in Application No. *08/964,236* .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☒ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☒ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____.
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

David Ton

DAVID TON
PRIMARY EXAMINER

1. The drawings are objected to because Fig. 15 is missing. Correction is requested.

2. Claims 1-7 and 10-16 are allowed.

3. The following is an Examiner's Statement of Reasons for Allowance:

a). The prior art of record teaches the claimed invention substantially, but it fails to teach or suggest singly or in combination a semiconductor integrated circuit device comprising a logic circuit, a SDRAM having a core unit and a SDRAM control circuit wherein the SDRAM control circuit receiving external control signals for said SDRAM from the logic circuit and outputting internal control signals to said core unit and the internal control signals control said core unit as set forth in independent claim 1. Claims 1-6 are allowed because of the combination of additional limitations and the limitation listed above.

b). The prior art of record teaches the claimed invention substantially, but it fails to teach or suggest singly or in combination a method for testing an SDRAM having a logic circuit and a core unit integrated into a single semiconductor chip by selecting the external test signals from the external input terminal using a selector, and providing the selected signals to the core unit of the SDRAM for testing wherein the external test signals are external control signals for the core unit and are decoded by a decoder to be the internal control signals provided to the selector as set forth in independent claim 7.

c). The prior art of record teaches the claimed invention substantially, but it

fails to teach or suggest singly or in combination a semiconductor integrated circuit device comprising a logic circuit, a RAM with a command decode system and a core unit integrated into a single semiconductor chip wherein a RAM control circuit receiving external control signals for said RAM from said logic circuit and outputting internal control signals for controlling said core unit of said RAM with the control decode system wherein the internal control signals control the core unit as set forth in independent claim 10. Claims 10-15 are allowed because of the combination of additional limitations and the limitation listed above.

d). The prior art of record teaches the claimed invention substantially, but it fails to teach or suggest singly or in combination a method for testing a RAM with a command decode system by using a selector, selecting external test signals from the external input terminal means and providing the selected signals to a core unit of said RAM with a command decode system for testing wherein the external test signals are external control signals for said core unit and are decoded by a decoder to be the internal control signals provided to said selector as set forth in independent claim 16.

4. Any comments considered necessary by applicant must be submitted no later than the payment of the Issue Fee and, to avoid processing delays, should preferably accompany the Issue Fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance".

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Ton whose telephone number is (571) 272-3828. The examiner can normally be reached on M-Th from 5:30 - 4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

David Ton
Primary Examiner
Art Unit 2133